

FIG. 1A

0	4 5		7 8	11 12	15 16	19 20	23 24	31
F	H		AM	T	S	R	0	

FIG. 1B

0	4 5		7 8	A22				29 30	31
F	H								BM

FIG. 1C

0	4 5		7 8	11 12	15 16	I16			31
F	H		CM	T					

FIG. 1D

0	4 5		7 8	11 12	15 16	19 20	TV12		31
F	H		P	T	S				

FIG. 1E

0	4 5		7 8	11 12	15 16	19 20	23 24	31
F	H		TM	T	S	R	SI8	

FIG. 1F

0	1	2	3	4	5	implementation dependent					31
1	1	1	1	1	1						

**FIG. 2**

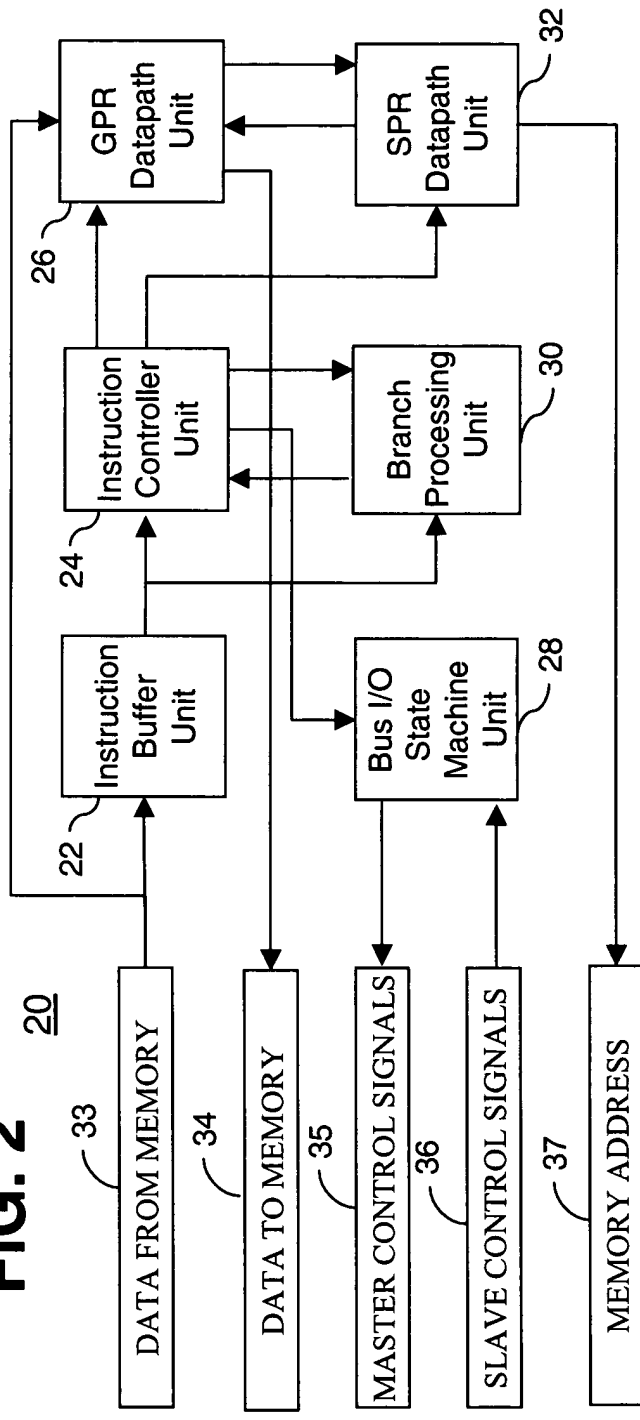


FIG. 3

40

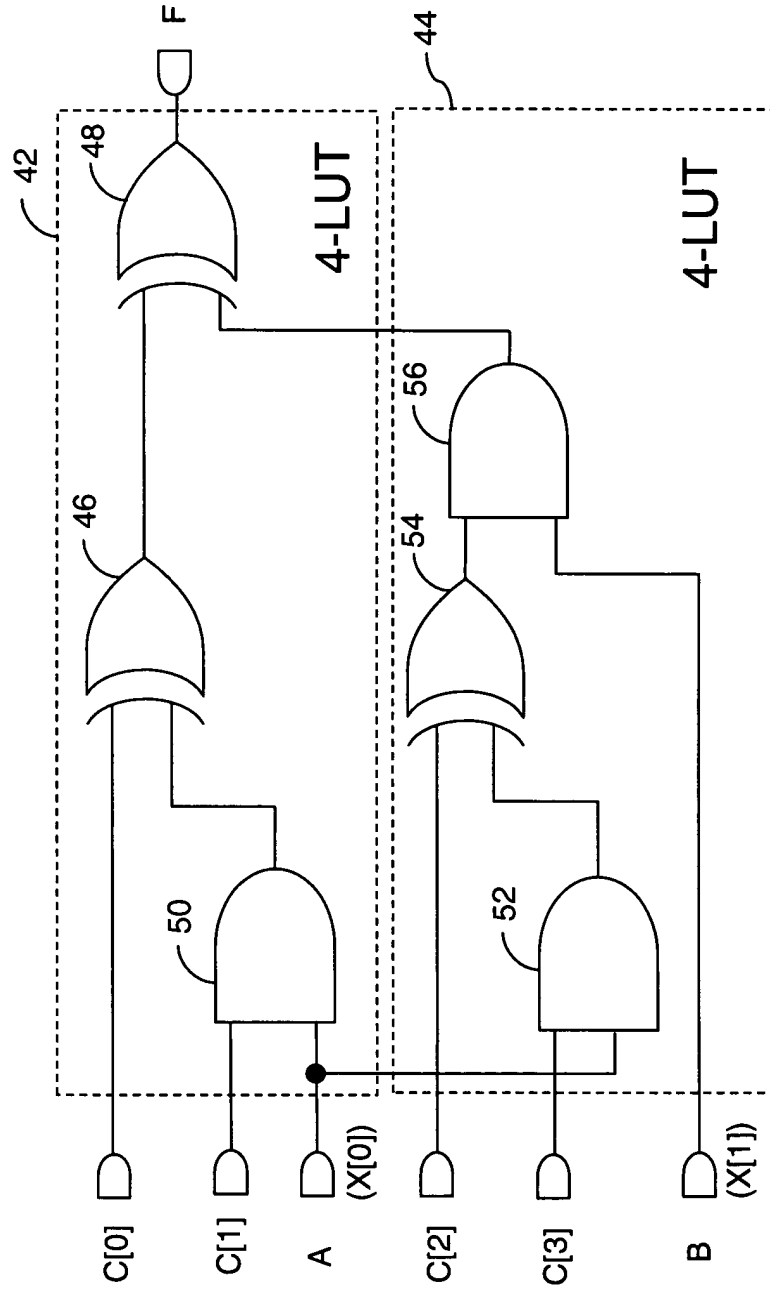
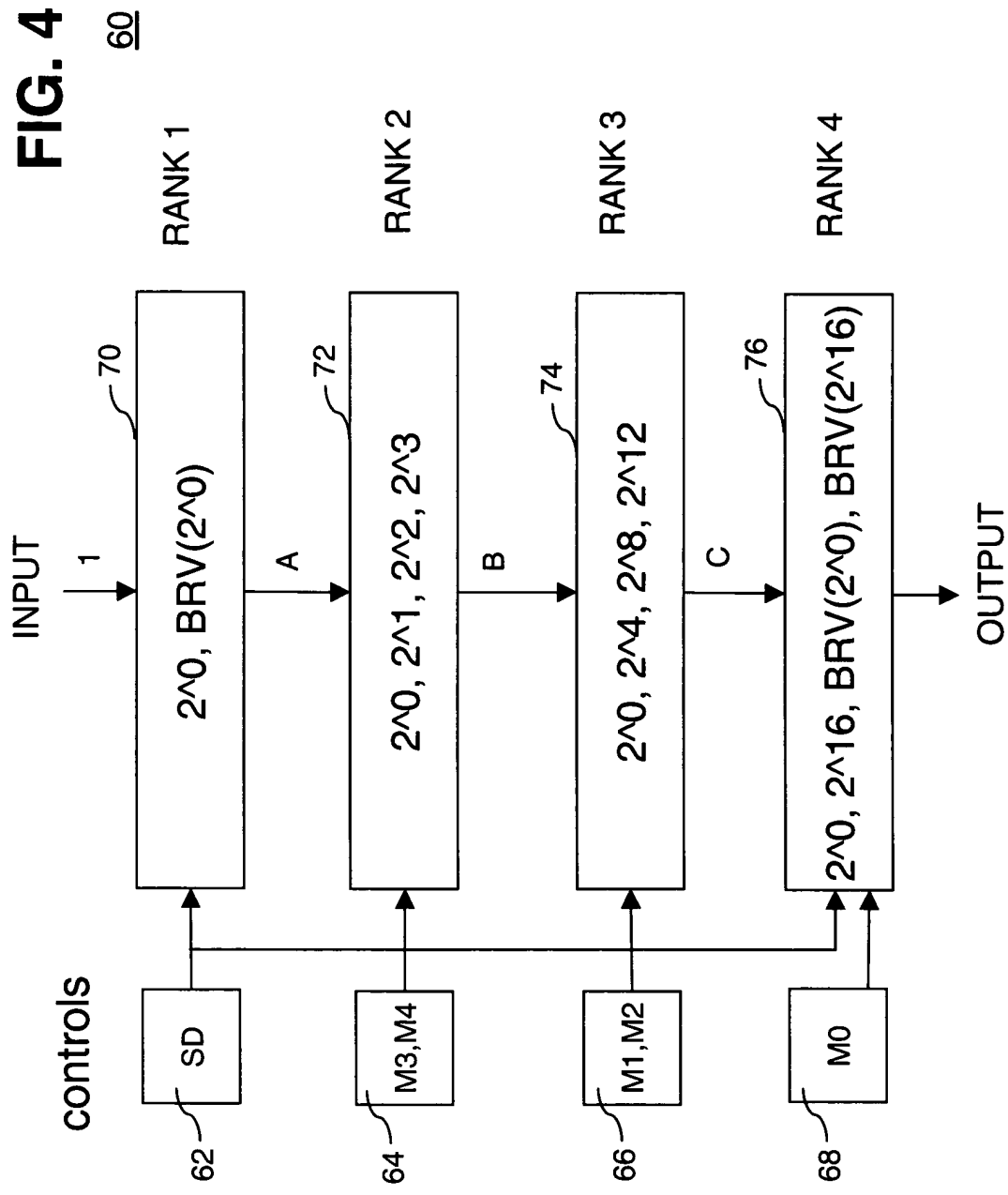


FIG. 4



**FIG. 5**

0	7	8	15	16	23	24	31
byte 3		byte 2		byte 1		byte 0	

**FIG. 6**

0	7	8	15	16	23	24	31
address + 0		address + 1		address + 2		address + 3	

**FIG. 7**

0	31
address	

**FIG. 8**

0	31
byte address	

**FIG. 9**

0	30	31
half-word address		
		X

**FIG. 10**

0	word address												29	30	31
														X	X

**FIG. 11**

0	instruction address												29	30	31
														0	0

**FIG. 12**

0	1	2	3	4	17				18	19	20	31			
N	V	C	Z		undefined				TE	IE		IV12			

**FIG. 13**

0	instruction from JTAG port												31		

**FIG. 14**

0	external data I/O via JTAG port												31		



FIG. 20

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
$l_0$	$l_0$	$l_1$	$l_1$	$l_2$	$l_2$	$l_3$	$l_3$	$l_4$	$l_4$	$l_5$	$l_5$	$l_6$	$l_6$	$l_7$	$l_7$	$l_8$	$l_8$	$l_9$	$l_9$	$l_{10}$	$l_{10}$	$l_{11}$	$l_{11}$	$l_{12}$	$l_{12}$	$l_{13}$	$l_{13}$	$l_{14}$	$l_{14}$	$l_{15}$	

FIG. 21

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
$l_0$	$l_0$	$l_0$	$l_0$	$l_0$	$l_0$	$l_0$	$l_0$	$l_0$	$l_0$	$l_0$	$l_0$	$l_0$	$l_0$	$l_0$	$l_0$	$l_0$	$l_1$	$l_2$	$l_3$	$l_4$	$l_5$	$l_6$	$l_7$	$l_8$	$l_9$	$l_{10}$	$l_{11}$	$l_{12}$	$l_{13}$	$l_{14}$	$l_{15}$

FIG. 22

0	1	2	3	4	5	7	8	11	12	15	16	31
1	0	0	1	1	H	CM		T		I16		



**FIG. 23**

<b>CM[0:3]</b>	<b>operation mode</b>	<b>bit mask mode</b>	<b>composite immediate instruction</b>
0000	and or xor add	fill low	imm_and_fill_low
0001		low	imm_or_low
0010		low	imm_xor_low
0011		low	imm_add_low
0100	and or xor add	fill high	imm_and_fill_high
0101		high	imm_or_high
0110		high	imm_xor_high
0111		high	imm_add_high
1000	and or xor add	dplx	imm_and_dplx
1001		dplx	imm_or_dplx
1010		dplx	imm_xor_dplx
1011		dplx	imm_add_dplx
1100	and or xor add	sign	imm_and_sign
1101		sign	imm_or_sign
1110		sign	imm_xor_sign
1111		sign	imm_add_sign